Monte Carlo simulation of double gate silicon on insulator devices operated as velocity modulation transistors

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We used an ensemble Monte Carlo simulator to study both the dc and transient behavior of a double gate silicon-on-insulator transistor (DGSOI) operated as a velocity modulation transistor (VMT) and as a conventional field effect transistor (FET). Operated as a VMT, the DGSOI transistor provides switching times shorter than 1 ps regardless of the channel length, with a significant current modulation factor at room temperature. The same device operated as a FET provides much longer switching times which, in addition, increase with the channel length. © 2005 American Institute of Physics. [DOI: 10.1063/1.1929085]

New end-user applications in the fields of wireless local area networks, medical imaging, civil security, automotive radars, and environmental monitoring (among others) need for their development electron devices running at very high frequencies (in the THz range). Up to now, these applications fall in the influence field of III–V technologies or compound silicon technologies (Si/SiGe). However, the possibility of using standard silicon manufacturing facilities to fabricate circuits running in the THz range would greatly increase the expectatives of these new applications for obvious reasons.

The switching time in a field effect transistor (FET) is mainly controlled by the transit time of the carriers from source to drain. In consequence, the transistor channel length needs to be reduced well below 100 nm in order to obtain transit times in the subpicosecond range and, therefore, devices working in the terahertz range. The fabrication of ultrashort gate FETs requires very expensive and advanced facilities. Moreover, such short devices confront fundamental physical limitations, known as short-channel effects, which prevent normal operation. In 1982, Sakaki introduced the concept of velocity modulation transistor (VMT), seeking to achieve devices free from transit time limitation, and therefore capable of switching in times of less than 1 ps regardless of the channel length. The concept of VMT exploits the ultrashort perpendicular transit time between two closely adjacent channels with very different transport properties, one channel having high electron mobility (high-mobility channel), and the other channel having very low electron mobility (low-mobility channel); thus, it is feasible to transfer all the charge from one channel to the other without significantly changing the total number of carriers in the device, i.e., neither of the channels is charged or discharged through the source or drain electrodes.

This device was originally proposed using different III–V heterostructures (double gate n-AlGaAs/GaAs heterojunction device and a resonantly coupled GaAs/AlGaAs double quantum well device). These structures have been extensively studied and even, very recently, fabricated using III–V technology. However, it would be very interesting to see whether this VMT concept could be applied in the context of silicon-based technology. Crow et al. have already simulated Si VMTs at low temperatures (T=77 K), showing that current can be switched between the low and high mobility regions of the channel within 1.5 ps.

The continuous advances and improvements in silicon-on-insulator (SOI) technology mean that the VMT concept is easily transferable to silicon technology. In fact, a double gate silicon-on-insulator transistor (DGSOI) could be operated as a VMT. If the two gates of a DGSOI device are simultaneously biased, two channels are formed near each Si/SiO2 interface (if the silicon is thick enough to avoid the volume inversion effect). However, if only one gate is biased (say, the front gate), while the other one (the back gate) is unbiased, only one channel is formed near the front gate Si/SiO2 interface. If we now exchange the biases applied to each gate, the electrons will be quickly transferred from one channel to the other, without changing the total inversion charge in the structure (i.e., it is not necessary to introduce or to extract carriers from the channel through source or drain electrodes). To achieve mobility modulation, the mobility in one of the two channels (the low mobility channel) must be strongly degraded. This degradation can be obtained, for example, by creating an artificial corrugation in the Si/SiO2 interface. Other approaches could be used to create the mobility degradation, such as high doping compensation in the back channel, or the use of amorphous silicon to build the degraded channel.

The aim of this work is to carry out a theoretical investigation into the switching times in these DGSOI devices operated as VMTs at room temperature, as a function of the channel length. An ensemble Monte Carlo (EMC) scheme was used to self-consistently solve the Poisson and the Boltzmann transport equations. As the main result, we show that it is possible to obtain switching times in the subpicosecond region for Si VMTs, regardless of the channel length, and with acceptable Ioff/Ion ratios even at room temperature.

Figure 1 shows the dc characteristics of a DGSOI transistor operated as VMT obtained by EMC simulation. The silicon thickness was considered to be Tw=20 nm, while the gate length was taken as LG=0.1 µm. The two oxide
layers were considered to be 10 nm thick. To achieve the current modulation (i.e., a low mobility channel (back channel) and a high mobility channel (front channel)) we considered the lower Si/SiO$_2$ interface to be affected by a greater roughness. We assumed Fuch’s model$^{16}$ to take into account surface roughness scattering with fully diffuse scattering at this interface, and specular scattering at the upper (high mobility) interface. In these conditions, the electron mobility in the low field high-mobility channel is around $\mu_n = 400$ cm$^2$/V s while $\mu_n = 10$ cm$^2$/V s in the low mobility channel. Solid lines correspond to the case when the upper high mobility channel is on and the lower low-mobility channel is off ($V_{FG} > 0$ V, $V_{BG} = -1$ V), while dashed lines correspond to the case where the current is exclusively due to the low-mobility channel, i.e., $V_{FG} = -1$ V, $V_{BG} > 0$ V. As shown in the figure, a current modulation factor greater than 40 is obtained.

We also studied the transient behavior of this device when it is operated as a VMT, that is to say, when carriers are transferred from the high mobility channel to the low mobility one and vice-versa to obtain the current modulation. Figure 2 shows the transient response of the device for different channel lengths. The number of particles considered in the simulation at any moment for the same devices is also shown. From 0 to 5 ps, the high mobility channel is on, while the low mobility channel is off ($V_{FG} = 1.5$ V, $V_{BG} = -1$ V). At $t = 5$ ps the polarization in both gates is switched, i.e., ($V_{FG} = -1$ V, $V_{BG} = 1.5$ V). Electrons are quickly transferred from the upper channel to the lower one, while the total electron concentration remains constant, as shown in the lower graph of Fig. 2. The new steady state level (low current level) is reached in less than a picosecond, even for the longer device ($L_m = 0.5$ $\mu$m). At $t = 10$ ps, gate voltages are switched again, and so the electrons are transferred again to the upper high mobility channel. Once more, the steady state is reached before 1 ps. As shown in Fig. 2, the number of particles (superparticles considered for the EMC simulation, which correspond to $5 \times 10^4$ electrons) in the devices also remains constant in this transition, which means it is not necessary to introduce or to remove charge through the source or drain electrodes when the transition is produced, but merely to transfer the electrons from one channel to the other. The procedure used to calculate the number of particles (superparticles indeed) is the standard one used in ensemble Monte Carlo simulations.$^{17}$ Initially the number of superparticles is assigned proportional to the electron distribution obtained from the self-consistent solution of Poisson and drift-diffusion equations which is considered as starting point. Then the number of particles is dynamically calculated in the EMC procedure taking into account the number of particles which leave the device through the drain or the source and imposing the maintenance of the charge neutrality in the vicinity of the source and drain ohmic contacts.$^{17}$

We also studied the behavior of this device when it works as a conventional FET device, that is to say, when current modulation is obtained by modifying the number of carriers in the channel. For the sake of comparison we have considered two situations: (a) single gate operation, SG: current conduction through only one channel (the upper one) while the lower channel is always fully depleted ($V_{BG}$ is always $-1$ V, which is below the threshold voltage, $V_{th}$); and (b) double gate operation, DG: current conduction simultaneously through the two channels (both gates are simultaneously biased at the same voltage). In both cases the back channel is considered to be non-degraded. In the SG mode the device is set on by biasing the upper gate (front gate) to $V_{FG} = 1.5$ V, and it is set off by turning $V_{FG}$ to $-1$ V (which is below $V_{th}$), i.e., as is done in a conventional FET. In the DG mode the device is set on by simultaneously biasing both gates to $V_{FG} = V_{BG} = 1.5$ V, and it is set off by turning both gates to $V_{FG} = V_{BG} = -1$ V.

Figure 3 shows the transient behavior of the device operated as a FET (both SG and DG modes) and as a VMT for different channel lengths. As can be seen, and contrary to the VMT behavior shown in Fig. 2, in both FET modes switching times strongly depend on channel lengths, and it is necessary for the channel length to be well below 0.1 $\mu$m to achieve switching times comparable to those obtained with the same device when operated in VMT mode. In the FET modes, to switch the device from the OFF to the ON state it is necessary to insert a large number of carriers into the channel from the source and drain electrodes, and this takes longer as the channel length increases. As expected, it is also observed that switching times are shorter in the DG mode than in the SG mode due to the simultaneous effect of the
two gates. This effect is more important as the channel length increases.

In summary, we show that it is possible to use the VMT concept in SOI technology. We used an EMC to study both the dc and the transient behavior of a DGSOI device operated as a VMT and as a conventional FET (SG and DG modes). We show that when operated as a VMT the DGSOI transistor provides switching times of less than 1 ps regardless of the channel length with a significant current modulation factor at room temperature. The same device operated as a FET provides longer switching times which increase with channel length, as expected.

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