Gate bias symmetry dependency of electron mobility and prospect of velocity modulation in double-gate silicon-on-insulator transistors

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We report on detailed room-temperature transport properties of a 17 nm thick double-gate silicon-on-insulator (DGSOI) transistor. We find that when the electron gas is transferred between the top and the bottom of the silicon-on-insulator (SOI) layer by changing the gate bias symmetry (i.e., applying the gate biases in a push–pull fashion), while keeping the carrier density constant the maximum mobility occurs when the electron gas symmetrically occupies the whole SOI slab. The observed mobility behavior is the fingerprint of volume inversion/accumulation. This gate bias symmetry dependency of the mobility suggests that DGSOI devices intrinsically can be operated in a velocity modulation transistor (VMT) mode. In the experimental gate bias window, the maximum velocity/mobility modulation is ~40%. The VMT transconductance exceeds conventional single-gate transconductance when electron density is above ~5.3 × 10^16 m^-2. Improvements of the observed VMT operation in thin DGSOI devices are discussed. © 2004 American Institute of Physics. [DOI: 10.1063/1.1829384]

Due to many advantages and full process compatibility in comparison with the conventional bulk Si-based devices silicon-on-insulator (SOI) technology is considered to be the future course of integrated circuit industry.1,2 In this framework, especially thin single-gate (SG) and double-gate (DG) SOI metal-oxide–semiconductor field-effect-transistor (MOSFET) structures are intensively explored at the moment. Both of these devices have many advantages over the standard bulk MOSFETs. However, DGSOI MOSFETs are usually regarded as the most promising solution to the problems faced when the device/gate length is downscaled into sub-50 nm regime (short channel effects). From the viewpoint of the short channel effects, the DGSOI is more effective in electrostatic gate control of the transistor channel charge in comparison to SGSOI.3 In addition to boosting the gate control, DGSOI also provides other benefits in the form of enhanced electron mobility.3,4 This enhancement is obtained in thin DGSOI transistors (SOI thickness ≤ 25 nm) in the volume inversion/accumulation regime where the electron gas occupies the whole SOI film. According to recent Monte Carlo (MC) simulations,5 the maximum enhancement occurs when the electron distribution is symmetric in the film.

In this letter, we report on the room-temperature electronic properties of a 17 nm thick DGSOI MOSFET device. The mobility and electron density are mapped in a large DG bias window enabling detailed investigation of the mobility behavior at different gate bias (electron distribution) symmetries. The mobility shows the expected enhancement and our experimental results further show that DGSOI transistors intrinsically have a possibility for velocity modulation transistor (VMT) operation. In this type of transistor, the channel current modulation is based on electron mobility modulation (MM) [or velocity modulation (VM)] at constant electron density, which leads to ultra-high speed operation that is not limited by the source–drain transit time.7 Even though the VM operation is not fundamentally determined by the absolute magnitude of the channel mobilities, it has been previously reported only in high mobility heterostructures (see, e.g., Ref. 8).

The DGSOI MOSFETs were fabricated on commercially available 100 nm unibond (100) SOI wafers. The nominal SOI film thickness was 400 nm and the buried oxide (BOX) was 400 nm thick. The initial donor concentration of the SOI film was ~10^21 m^-3. First, we exchanged the n^- handle wafer to an n^+ wafer to enable efficient metallic back gating at all temperatures. This procedure began by a growth of a 80 nm thick dry oxide at 1000 °C. Then, the SOI wafer was vacuum bonded to an n^+ (111) Si wafer with 2 × 10^25 m^-3 arsenic concentration. The bonded interface was annealed at 1100 °C and the whole handle wafer was etched in 25% tetramethyl ammonium hydroxide. Finally the “old” BOX layer was stripped in a 10% HF and as a result we had a SOI wafer with heavily doped handle, 360 nm thick SOI film, and 80 nm thick BOX (back gate oxide). The actual device fabrication and SOI film thickness mapping measurements were performed following the procedures described in detail in Ref. 9. Figure 1 shows a transmission electron microscope (TEM) image of a DGSOI test structure that was processed on the same SOI wafer as the transistors used in the experiments. The DGSOI transistors have a maximum 4.2 K (Hall) mobility of 1.9 m^2/V s, which is a signature of high-

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FIG. 1. TEM image of 18 nm thick DG test structure and schematic illustration of gate biasing in the experiments.
MOSFET Hall bar structure

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thickness \( t_{SOI} = 17.3 \text{ nm} \), gate oxide thickness \( t_{OX} = 43 \text{ nm} \), and BOX (back gate oxide) thickness \( t_{BOX} = 80 \text{ nm} \). The mobility

\( \mu = \frac{G_s}{G_{s,max}} \), where \( G_s \) is the schect conductance obtained from a four-point measurement. We used Agilent 4294A precision impedance analyzer at a frequency of 691 Hz in the SCV measurements. This frequency was low enough to provide results that were independent of the channel charging delays, when all the voltage probes and the source and the drain were connected to the virtual ground of the analyzer.

Figure 2(a) shows constant mobility (black thin curves) and electron density (dashed thick gray curves) contours measured as a function of top gate voltage \( V_{TG} \) and back gate voltage \( V_{BG} \) at 300 K. The family of curves explicitly shows how the electron mobility behaves as a function of carrier density at different gate bias symmetries. We can see that on any of the constant \( N \) contours, the mobility is the higher the closer the gate biases are to the symmetric gate bias line \( V_{TG}/t_{OX}=V_{BG}/t_{BOX} \) [dashed black line in Fig. 2(a)]. When gate bias asymmetry is increased, the mobility decreases monotonically. This is depicted more clearly in Fig. 2(b) where the relative sheet conductance \( G_s/G_{s,max} \) is equal to the relative mobility \( \mu/\mu_{max} \), is presented along constant electron density contours as a function of top gate voltage change \( \Delta V_{TG} = V_{TG} - V_{TG,SYM} \) at different \( N \) (\( V_{TG} = V_{TG,SYM} \) corresponds to \( V_{TG}/t_{OX}=V_{BG}/t_{BOX} \)). The difference between symmetric gate bias mobility (\( \Delta V_{TG} = 0 \)) and top interface SG mobility (\( V_{BG}=0 \)), which is indicated with circles in Fig. 2, is in agreement with MC simulations and recent experiments.

The symmetric gate bias \( \Delta V_{TG} = 0 \) corresponds to the case where the electron gas occupies symmetrically the whole SOI film. When asymmetric bias is applied (\( \Delta V_{TG} \neq 0 \)), the electron gas is moved from the symmetric position toward the SOI–top gate oxide or SOI–BOX interfaces. The symmetric case is depicted in Fig. 3(a), which shows self-consistently calculated electron distribution \( n(z) \) at different \( N \). The figure shows the ratio \( \text{min/} \mathbf{max} \) and the distribution in the SOI film

FIG. 2. (a) Experimental electron mobility \( \mu \) (black thin contours) and density \( N \) (thick dashed gray contours with gray bold labels) as a function of top gate voltage \( V_{TG} \) and back gate voltage \( V_{BG} \) of a 17.3 nm thick DGSOI MOSFET at 300 K. The contour spacing for \( \mu \) and \( N \) are 0.2 \( \times 10^{-2} \text{ m}^2/\text{Vs} \) and 1.0 \( \times 10^{16} \text{ m}^{-2} \), respectively. The dashed black line is the symmetric gate bias line \( V_{TG}/t_{OX}=V_{BG}/t_{BOX} \) (b) Relative sheet conductance (mobility) modulation \( G_s/G_{s,max} \) along constant electron density contours as a function of top gate voltage change \( \Delta V_{TG} \). \( \Delta V_{TG}=0 \) V corresponds to the black dashed line in (a) and the circles indicate points where \( V_{BG}=0 \).

FIG. 3. (a) Self-consistently calculated quantum mechanical electron distribution in the SOI film (\( t_{SOI}=17.3 \text{ nm} \)) at different electron density values \( (N=1,2,4,6 \times 10^{16} \text{ m}^{-2} \) from bottom to top) at \( \Delta V_{TG}=0 \) V at 300 K. The calculations were performed for 12 subbands within the Hartree approximation. (b) Ratio \( \text{min/} \mathbf{max}=n(t_{SOI}/2)/\mathbf{max}[n(z)] \) vs electron density.
In order to get a quantitative estimate of the magnitude of the VMT transconductance, we will compare it with SG transconductance. In the case of a DG device that is operated in a VMT mode, a small signal excitation is divided between the two gates in such a way that the electron density remains constant. Thus, the DG transconductance should be defined as a directional derivative of the channel current in the $V_{TG}^{-}V_{BG}$ plane of Fig. 2(a). The experimental data presented in this work are in the low-field linear regime and, therefore, we confine ourselves to study transconductance of one square. The current through one square is $I_s = G_s V_{ds}$ (sheet conductance, $V_{ds}$ voltage over one square) and the DG transconductance of one square $g_{m,s} = \mathbf{u} \cdot \nabla V_{ds}$, where $G_s$ is the gradient operator and $\mathbf{u}$ is an arbitrary unit vector, which chooses the direction, in the $V_{TG}^{-}V_{BG}$ plane. In the linear regime, the magnitude of $V_s$ is irrelevant and it is convenient to study normalized transconductance

$$g = g_{m,s}/V_s = \mathbf{u} \cdot \nabla G_s. \quad (1)$$

Vector $\mathbf{u}$ along the direction of constant $N$ contour, i.e., $\mathbf{u} \perp \nabla N$, corresponds to the velocity modulation transconductance $g = g_{VMT}$. When $\mathbf{u}$ is equal to the unit vectors $\mathbf{u}_{TG}$ or $\mathbf{u}_{BG}$ of the $V_{TG}^{-}V_{BG}$ plane, Eq. (1) reduces to the SG case $g = g_{SG} = \partial G_s/\partial V_{TG,BG}$. Figure 4 shows $g_{VMT} (\mathbf{u} \perp \nabla N)$ and $g_{SG}$ ($\mathbf{u} = \mathbf{u}_{TG}$) and their ratio as a function of top gate voltage and electron density at 300 K. Back gate is set to 0.56 V because $g_{VMT}$ reaches its maximum at this $V_{BG}$ value (above threshold and close to $V_{BG} = 0$ $g_{SG}$ has a negligible dependency on $V_{BG}$). The data are calculated from experimental $G_s$ and in order to symmetrize the device, we have used the substitution $V_{BG} \rightarrow t_{OX}/t_{BOX} V_{BG}$ in Eq. (1). The SG transconductance shows the typical behavior where it has a maximum close to threshold and monotonically decreases at higher $V_{TG}$ values. Whereas, the behavior of $g_{VMT}$ is the opposite with a monotonic increase as a function $V_{TG}$. Already at $V_{TG} \sim 1.0$ V ($N \sim 0.7 \times 10^{16}$ m$^{-2}$), it is more than 10% from $g_{SG}$ and $g_{VMT} \gg g_{SG}$ when $V_{TG} \geq 10.8$ V ($N \leq 5.3 \times 10^{16}$ m$^{-2}$). The difference between $g_{VMT}$ and $g_{SG}$ in Fig. 4 obviously follows from the fact that the VMT transconductance is proportional to one term $g_{VMT} \propto \mathbf{u} \cdot \nabla \mu \left( \mathbf{u} \cdot \nabla \mu \right) > 0, \mathbf{u} \perp \nabla N)$, while $g_{SG} \propto N \partial \mu / \partial V_{TG} + \mu \partial N / \partial V_{TG}$ and at high electron densities these two terms have opposite sign.

The above results show that at some gate voltage bias regions, we are able to observe comparable or even higher transconductance (and, therefore, higher gain) in the VMT operational mode than in SG mode. Unfortunately, the magnitude of the MM is rather low, which suggests that the demonstrated operation may not be directly suitable for applications. However, it should be noted that the demonstrated VMT operation is purely an intrinsic property of thin DGSOI MOSFETs and the VMT transconductance of Fig. 4 follows mainly from the gate bias symmetry dependency of phonon and surface roughness scattering. Undoubtedly, the VMT effect in a DGSOI device can be improved with a proper design. An especially attractive path in improving the VMT operation would be to intentionally roughen either the BOX–SOI or gate oxide–SOI interface. In this approach, the current modulation is obtained by moving the electron gas between the roughened and smooth interfaces. According to preliminary MC simulations of a 20 nm thick DGSOI VMT structure, the roughening method would lead to maximum/minimum mobility ratio that exceeds 10 at high carrier densities. This is certainly a value that is more than enough for applications. Realization and characterization of this type of SOI structure will be a task for future experimental investigations.

In summary, we have reported on detailed room-temperature mobility and electron density measurements of a 17 nm thick DGSOI MOSFET. We demonstrated that when the electron gas is moved between the top and the bottom of the SOI layer by changing the gate bias symmetry (i.e., applying the gate biases in a push–pull fashion) while keeping the carrier density constant, the maximum mobility occurs when the electron gas symmetrically occupies the whole SOI slab. When the electron gas is transferred from the symmetric position toward the SOI–top gate oxide or SOI–BOX interface, the mobility decreases monotonically. This behavior persists throughout the experimental electron density regime ($\sim 0.5 \times 10^{16}$ m$^{-2}$) and it is the fingerprint of volume accumulation. Physically, the phenomenon follows mainly from the gate bias (electron distribution) symmetry dependency of phonon and surface roughness scattering. The gate bias symmetry dependency of the mobility suggests that DGSOI devices intrinsically have a possibility for VMT operation. The VMT transconductance exceeds conventional SG transconductance when electron density is above $\sim 5.3 \times 10^{16}$ m$^{-2}$.

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