Electron mobility in extremely thin single-gate silicon-on-insulator inversion layers

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Inversion-layer mobility has been investigated in extremely thin silicon-on-insulator metal–oxide–semiconductor field-effect transistors with a silicon film thickness as low as 5 nm. The Poisson and Schrödinger equations have been self-consistently solved to take into account inversion layer quantization. To evaluate the electron mobility, the Boltzmann transport equation has been solved by the Monte Carlo method, simultaneously taking into account phonon, surface-roughness, and Coulomb scattering. We show that the reduction of the silicon layer has several effects on the electron mobility: (i) a greater confinement of the electrons in the thin silicon film, which implies an increase in the phonon-scattering rate and therefore a mobility decrease; (ii) a reduction in the conduction effective mass and the intervalley-scattering rate due to the redistribution of carriers in the two subband ladders as a consequence of size quantization resulting in a mobility increase; and (iii) an increase in Coulomb scattering because of a greater number of interface traps in the buried Si–SiO₂ and to a closer approach of these charged centers to the mobile carriers. The dependence of these effects on the silicon-layer thickness and on the inversion-charge concentration causes the mobility to be a nontrivial function of these variables. A detailed explanation of the mobility behavior is provided. Mobility for samples with silicon thickness below 10 nm is shown to increase in an electric field range that depends on the charged center concentration, while for silicon layers over 10 nm mobility always decreases as the silicon-layer thickness is reduced. © 1999 American Institute of Physics.

I. INTRODUCTION

Despite the numerous advantages of silicon-on-insulator (SOI) devices over their conventional bulk-silicon counterparts (in particular, with respect to radiation tolerance, lower parasitic capacitance, and short-channel effects)1, SOI technology has, until now, been considered a technology of the future. The constant improvements in conventional silicon technology have successively postponed the introduction of future. This has, until now, been a technology of the future. The constant improvements in conventional silicon technology have successively postponed the introduction of thin-film SOI technology in the device fabrication arena. However, nowadays, the high cost of state-of-the-art manufacturing facilities originated by the continuous scaling down of device dimensions are bringing about a change in this picture.² The main reason for these changes is related to the fact that SOI technology is fully compatible with existing manufacturing facilities, and that due to the use of an insulating substrate, it can significantly reduce the number of steps in the device fabrication process. Thus, thin-film SOI technology could help to control the rising costs of future technologies.³–₆

Therefore, due to their possible future applications, it is of great interest to characterize the performance of extremely thin SOI metal–oxide–semiconductor field-effect transistors (MOSFETs). In particular, electron mobility is one of the most important factors in determining MOS device characteristics, and therefore several groups have already experimentally studied the behavior of this parameter in such devices. It has recently been reported, for instance, that, down to 50 nm silicon-film thickness, the inversion-layer mobility of SOI MOSFETs is independent of the thickness of the silicon film,⁴ behaving universally regardless of the impurity doping concentration (as the bulk MOSFET mobility does). However, as the Si film becomes thinner, very different behavior is observed. The influence of Si-film thickness on electron mobility has been experimentally studied by different authors⁷–⁹ on high-quality SOI transistors built on silicon layers as thin as 8 nm, demonstrating a gradual mobility decrease when the silicon-film thickness is reduced below 20 nm. Different explanations have been provided for the mobility decrease as the silicon-film thickness shrinks:

Choi et al.⁸ attribute the mobility reduction to an increase in the lattice defects in the extremely thin silicon film sandwiched between two oxides as a consequence of the difference in the thermal-expansion coefficients between silicon and oxide. Nonetheless, although there is, in fact, an increase in stress in a thin silicon film, as shown by the parasitic bipolar current gain measured by the GIDL current method,⁶,¹⁰ this stress is too small to entirely justify the mobility reduction found experimentally.

Toriumi et al.⁹ attributed the mobility degradation to an increase in the Coulomb scattering rate in thinner SOI MOSFETs as a consequence of an increase in the interface trap density Nᵢᵢ in the back interface (buried oxide). In addition, as the silicon film is diminished, the distance between electrons and traps is also reduced, thus increasing Coulomb scattering and decreasing electron mobility. These research-

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ers have also studied the contribution of the internal strain in SOI using microscope Raman spectroscopy for various SOI thicknesses. They concluded that a small strain might affect the mobility at room temperature, although only slightly. Moreover, in their study on low-temperature properties, these authors claimed that no phonon contribution to the mobility degradation in thin SOI MOSFETs should be expected. They supported this statement by comparing the experimental Hall mobility in 5 nm SOI MOSFETs with the experimental Hall mobility on bulk MOSFETs, showing that electron mobility in SOI MOSFETs is much lower, whereas at 4.2 K no phonon contribution should exist. However, this result only proves that Coulomb scattering due to the buried-oxide trapped charge increase is one of the effects that contributes to degrading the mobility, but does not serve to discard a phonon contribution to the mobility degradation at higher temperatures.

Price et al.\textsuperscript{11} showed that the phonon-scattering rate increases as the confinement of electrons increases. This is because the less localized in the wave vector space the electrons are, the more phonons can assist in carrier transitions, and therefore the greater the scattering rate. This is why the phonon-limited mobility in a conventional MOSFET decreases as the transverse effective field increases.\textsuperscript{12} In the present study, if the top silicon film is thinner than a determined value, the confinement of electrons in the inversion layer increases (for a fixed transverse effective field) as the silicon film thickness decreases.\textsuperscript{13,14} Therefore a contribution of phonon scattering to the mobility reduction as the silicon film thickness diminishes is also expected.

Abramo et al.\textsuperscript{15} have theoretically studied the mobility behavior in very thin single- and double-gate SOI MOSFETs, but without taking into account the effect of Coulomb scattering and surface-roughness scattering. Nonetheless, they found that the phonon-limited mobility is a nontrivial function of the silicon thickness, since two competing mechanisms coexist: (i) the reduction of the silicon thickness increases the quantization and decreases the available density of states, leading to a mobility enhancement; (ii) when the silicon layer is decreased, instead, greater surface confinement of the wave functions occurs. This leads to an increase in the overlap factors and therefore of the scattering rates and, consequently, to a decrease in mobility.

Finally, in an extensive work, Shoji et al.\textsuperscript{13,14} predicted that the electron mobility in SOI inversion layers with silicon layers thinner than a given value $T_{\text{inv}}^{\text{th}}$ should behave differently than the one observed in bulk silicon inversion layers, $T_{\text{inv}}^{\text{th}}$ is the highest silicon thickness at which the condition $T_{\text{w}} < T_{\text{inv}}^{\text{th}}$ is fulfilled ($T_{\text{w}}$ being the top silicon-layer thickness, $T_{\text{inv}}$ the inversion region thickness, and $T_{\text{bulk}}^{\text{th}}$ the inversion-layer thickness in a bulk MOSFET for the same inversion-charge concentration). For $T_{\text{w}}$ less than $T_{\text{inv}}^{\text{th}}$, there is no equivalence between the electron states in the SOI and bulk silicon-inversion layers (for a fixed transverse electric field value). Therefore, as the electronic states are different, a different mobility value is expected, since electron mobility is completely governed by the electronic states of the inversion layer.

In summary, both experimental evidence and theoretical studies indicate a nontrivial behavior of electron mobility in ultrathin SOI MOSFETs. In this work we have theoretically analyzed the electron-transport properties in ultrathin SOI inversion layers and their dependence on the silicon-layer thickness and the inversion-charge concentration. To do so, we have numerically simulated these devices solving the Boltzmann transport equation (BTE) by the Monte Carlo method. Although there are several ways to solve the BTE,\textsuperscript{16} we have chosen to use the Monte Carlo method. This choice is based on the fact that the Monte Carlo method is thought to contain a more rigorous description of the physical phenomena involved in carrier transport than the methods based on the balance transport equations.

Electron quantization in the silicon inversion layer has been properly taken into account by self-consistently solving the Poisson and Schrödinger equations.\textsuperscript{13,14} The effect of reducing the silicon film thickness $T_{\text{w}}$ on the electron distribution in the inverse layer is carefully analyzed in Sec. II. In Sec. III, the Monte Carlo simulator is shown to be viable for calculating electron mobility curves and explaining their behavior as $T_{\text{w}}$ decreases. Finally, the main conclusions of this work are summarized in Sec. IV.

II. NUMERICAL SIMULATION

The structure we have studied consists of an undoped (100) silicon film sandwiched between two oxide layers. The gate-oxide thickness was taken as 5 nm, while the buried oxide was considered to be 80 nm thick. A silicon substrate was assumed under the buried oxide. A P⁺ poly gate was employed. Different thicknesses of the silicon film $T_{\text{w}}$, ranging from 50 to 5 nm, were considered.\textsuperscript{8,9} To accurately evaluate the electron distribution in the structure for a given voltage applied between the gate and the substrate, we must self-consistently solve the Schrödinger and Poisson equations. For the sake of simplicity, calculations are made in the Hartree approximation. Although this approximation can have serious drawbacks, the results obtained in its approach do not significantly alter when the more complicated calculation procedure necessary to take into account many-body effects is used. (For a detailed discussion of this issue see Refs. 17–19.) To solve Poisson’s equation we have considered a nonuniform adaptive mesh, employing an iterative Newton scheme. The actual band bending through the whole structure and the finite height of the barrier at the Si–SiO₂ interfaces have been considered. A simple nonparabolic band model for the silicon has been taken into account assuming $\alpha = 0.5 \ eV^{-1}$; $\alpha$ being the parameter of nonparabolicity. This limits our study to low-electron energies (below 0.5 eV). The procedure to obtain the solution of the Schrödinger equation for nonparabolic bands can be found elsewhere.\textsuperscript{20}

The electron effective masses are assumed to be those obtained for the silicon bulk.\textsuperscript{21} One may well question the use of effective-mass approximation for electronic states whose spatial extent is limited to a few atomic layers ($T_{\text{w}}$ less than 10 nm). As pointed out by Ando et al.\textsuperscript{17} it is thought to be the lack of knowledge about the physical parameters and uncertainties of the problem, rather than the effective-mass
approximation itself, that limits the accuracy of phononlimited electron mobility calculations. A detailed description of the self-consistent solution of the Poisson and Schrödinger equations can be found elsewhere.\textsuperscript{22–25}

From the self-consistent solution of the Poisson and Schrödinger equations, the following facts have been obtained.

(a) An important effect caused by the reduction of the silicon film thickness is the subband modulation effect. This effect is related to the split of the degeneracy of the Si conduction-band minima. As a consequence of the size quantization in the (100) silicon inversion layer, the degeneracy in the Si conduction-band minima breaks and the electrons are distributed into two ladders of subbands: one ladder arises from the two valleys showing the longitudinal mass $m_l$ in the direction perpendicular to the interface $(E_0, E_1, \ldots)$ and the other one from the four equivalent valleys showing the transverse mass $m_t$ in the same direction $(E'_0, E'_1, \ldots)$.$^{17,26}$ Since, in silicon, the longitudinal effect mass is greater than the transverse effective mass, the energy levels of the first ladder are lower than the energy levels of the prime ladder, i.e., $E_0 < E'_0, E_1 < E'_1$, etc.$^{12,26}$ On the other hand, the population of each subband $N_i$ is given by the following expression:\textsuperscript{17}

\[ N_i = \frac{k_B T}{\pi h^2} g_{vi} m_{di} \ln \left[ 1 + e^{(E_F - E_i)/k_B T} \right], \]  

where $k_B$ is the Boltzmann constant, $E_F$ is the Fermi level, $m_{di}$ is the density-of-states effective mass ($m_{di} = m_t$ for the nonprime ladder, and $m_{di} = \sqrt{m_t m_l}$ for the prime ladder), and $g_{vi}$ is the degeneracy of the valley ($g_{vi} = 2$ for the nonprime ladder and $g_{vi} = 4$ for the prime ladder). According to Eq. (1), the subband population depends on: (i) the separation between the Fermi level and the subband energy level, (ii) the degeneracy of the valley considered $g_{vi}$, and (iii) the density-of-states effective mass $m_{di}$. As a consequence of these dependencies, although $E_0 < E'_0$, and therefore $E_F - E_0 > E'_F - E'_0$, the greater degeneracy and the greater $m_{di}$ of the prime ladder makes it possible for $N_0 < N'_0$, if the separation $E'_0 - E_0$ is not overly great (as happens in bulk silicon-inversion layers at room temperature for low inversion-charge concentrations).\textsuperscript{17} As the conduction effective mass for electrons in nonprime subbands is equal to $m_c = m_l$, while the conduction effective mass for electrons in prime subbands is equal to $m'_c = 2m_l m_t/(m_l + m_t)$, this implies that $m'_c > m_c$. Therefore, the higher the population of prime subbands, the lower the average conduction effective mass, and therefore the lower the mobility.

Keeping in mind the above reasoning, in order to improve the electron-transport properties in silicon inversion layers, one should try to reduce the population of prime subbands, thus decreasing the electron conduction effective mass and at the same time increasing the electron mobility. To do so, according to expression (1), the subband energy difference between nonprime and prime subbands, i.e., $E'_0 - E_0$, should be increased.\textsuperscript{27} As shown below this can be achieved in ultrathin SOI inversion layers by reducing the silicon film thickness.

The self-consistent solution of the Poisson and Schrödinger equations in the structure described above demonstrates that the separation between the energy levels of the two subband ladders depends on the thickness of the silicon layer. This can be seen in Fig. 1, where the energy separation between the ground subband of each ladder is shown versus the silicon layer thickness for different sheet electron concentrations. Note that, while the inversion-charge distribution $T_{inv}$ is thinner than the silicon layer thickness $T_w$, the difference $E'_0 - E_0$ remains constant. However, as the silicon layer shrinks and becomes thinner than the bulk inversion layer ($T_w < T_w^{bulk}$), the difference $E'_0 - E_0$ begins to increase. An important consequence of this fact is that the population of nonprime subbands increases at the expense of the prime subband population as the silicon layer thickness is reduced. This effect can be clearly observed in Fig. 2, where the relative population of the ground subband of each ladder is shown versus the transverse effective field $E_{EFF}$ (as defined in Refs. 28 and 29) for two different silicon layer thicknesses $[T_w = 10 \text{ nm} \text{ (dashed line)}$ and $T_w = 5 \text{ nm} \text{ (solid line)}$. For $T_w = 10 \text{ nm}$, most of the electrons populate the ground subband of the prime ladder at low effective fields (and therefore at low inversion-charge concentrations), and only a high effective fields (at high inversion-charge concentrations) is the nonprime ladder more populated than
the nonprime one. This means that in this case \( T_w = 10 \) nm most of the electrons have a conduction effective mass equal to \( m_c' \). However, for \( T_w = 5 \) nm, the majority of the electrons populate the nonprime ladder in all the inversion-charge concentration range, thus showing a conduction effective mass equal to \( m_c \). Therefore, as \( m_c' > m_c \), a reduction in the conduction effective mass occurs as \( T_w \) is reduced. The reduction of the conduction effective mass of electrons as the silicon layer thickness decreases can clearly be observed in Fig. 3, where the average conduction effective mass versus the effective field for different silicon layer thicknesses is shown.

This redistribution of the inversion electrons as the silicon layer shrinks has, in addition, another important effect: the reduction of the intervalley scattering rate between non-equivalent valleys (\( f \) scattering) due to the greater separation of the energy levels related to prime subbands with respect to the unprime ones as the silicon film thickness is reduced.\(^{21,30–32} \)

We should call the reader’s attention to the fact that these two effects (reduction of the conduction effective mass and reduction of the intervalley scattering rate) are the same two that appear in strained silicon inversion layers built on \( Si_{1-x}Ge_x \) substrates (but in this case, as a consequence of the strain). As is known, the strain in the silicon layer produced by the different lattice constants between Si and \( Si_{1-x}Ge_x \) also causes the split of the sixfold degeneracy in the Si conduction-band minimum. The strain causes the sixfold degenerative valleys to separate into two groups: two lowered valleys with the longitudinal mass axis perpendicular to the interface and four raised valleys with the longitudinal mass axis parallel to the interface.\(^{32,33} \) This circumstance causes the redistribution of the inversion electrons, which mainly populate the subbands of the nonprime subbands.

(b) Another important effect that appears in SOI inversion layers as the silicon layer thickness is reduced is an increase in the phonon-scattering rate. In the case of silicon films thinner than 20 nm, the film \( T_w \) is thinner than the width of the inversion charge in bulk inversion layers for the same inversion-charge concentration \( T_{inv}^{bulk} \). This means that the electron confinement in ultrathin SOI inversion layers is greater than in bulk-inversion layers.\(^{13} \) That is, the uncertainty in the location of the electrons in the direction perpendicular to the interface is less in SOI samples than in bulk samples. In accordance with the uncertainty principle, there is a wider distribution of the electron’s momentum perpendicular to the interface. In other words, due to size quantization, the electron’s interface-directed momentum does not have a single value [as in three-dimensional (3D) electrons], but a distribution of likely values that expands as the silicon layer thickness is reduced. Taking into account the momentum conservation principle, there are more bulk phonons available that can assist in transitions between electron states, and therefore an increase in the phonon-scattering rate is expected. As a consequence, the same inversion-charge concentration, the phonon-scattering rate is greater in thinner films than in thicker ones (since the confinement is greater), and therefore a mobility reduction can be expected. A more comprehensive explanation about the behavior of phonon-limited mobility in ultrathin SOI inversion layers with silicon layer thicknesses down to 10 nm can be found in Refs. 34 and 35 (and references therein).

The conclusions in points (a) and (b) indicate that two opposite trends appear in the electron mobility as the silicon layer thickness is reduced. It would be interesting to know which of these trends, if either, is dominant, and whether there is a critical silicon layer thickness at which a change in the mobility behavior is observed; that is to say, whether a change is produced in the trend of the electron mobility as the silicon layer thickness is reduced.

III. ELECTRON MOBILITY CALCULATION

To study the electron mobility behavior in ultrathin single-gate SOI inversion layers we have used a one-electron Monte Carlo simulator\(^ {22–24} \) since the Monte Carlo method allows a more rigorous description of device physics than models based on the solution of fundamental balance equations.

Phonon, surface-roughness, and Coulomb scattering have been taken into account in this work. For the phonon scattering, we have considered acoustic deformation potential scattering and intervalley phonon events (both between equivalent and nonequivalent valleys). The coupling constants for the intervalley phonons and the acoustic deformation potential were the same as in the bulk silicon inversion layers.\(^ {19,21} \) The phonon-scattering rates for inversion layers have been deduced by using Price’s formulation.\(^ {11} \) Here again, the use of bulk phonons is questionable, as the presence of Si–SiO\(_2\) interfaces undoubtedly alters the dispersion of the phonons, their nature, and their coupling to the electrons. Previous studies\(^ {26} \) taking these effects into account under very idealized conditions showed that phonon-limited mobility is reduced by 20% or less\(^ {19} \) due to the presence of the Si/SiO\(_2\) interface. Nevertheless, if such idealized conditions are relaxed, an even lesser reduction is expected. Therefore, and due also the difficulty of dealing with the effects of the interfaces on the phonon-scattering rate,\(^ {19,36} \) we have ignored such effects, considering only that bulk phonons are not influenced by the layered structure. In any case, the presence of both Si/SiO\(_2\) interfaces is even more important as the silicon layer thickness is reduced. As shown below, this indicates a further reduction in the phonon-
limited mobility as the silicon-layer thickness decreases. Finally, the effect of SiO2 polar-phonon scattering has also been ignored.

In our simulation the electron energy has been limited to 0.5 eV, since for higher electron energies the results obtained by the simulation are not likely to be very accurate, as a detailed band structure was not used. Accordingly, as the silicon band gap is set to 1.12 eV at room temperature (and therefore this sets the energy threshold for the impact ionization process), impact ionization has not been included.

Using this simulator, we have calculated the electron mobility in single-gate SOI inversion layers for different silicon film thicknesses $T_w$. Our attention has been focused on the evaluation of the stationary drift velocity and the low-field mobility. A comprehensive description of this simulator can be found elsewhere.22–24

Figure 4 shows electron mobility curves versus the transverse effective field for different silicon-layer thicknesses calculated at room temperature taking into account only phonon and surface roughness scattering. We have assumed that the two Si–SiO2 interfaces have the same surface-roughness parameters ($\Delta = 0.2$ nm, $L = 1.5$ nm). To take into account the effect of surface-roughness scattering a new model has been developed.29

A study of Fig. 4 reveals the following circumstances.

(a) At low inversion-charge concentrations the electron mobility decreases as $T_w$ decreases even for the thinner sample [$T_w = 5$ nm (dashed line)]. Moreover, at low inversion-charge concentrations, phonon scattering is the dominant scattering mechanism (in the absence of Coulomb scattering as is the case here). The mobility behavior shown in Fig. 4 demonstrates that, of the two effects discussed in Sec. II, the increase in phonon scattering is the dominant effect at low inversion-charge concentrations for all the silicon thicknesses considered.

(b) However, at high inversion-charge concentrations (or high transverse effective fields), where phonon scattering is not the main scattering mechanism yet, the electron mobility decreases as $T_w$ is reduced down to 10 nm (as a consequence of the phonon-scattering rate increase). However, for thinner silicon layers the opposite effect is observed, as a consequence of the reduction of the conduction effective mass, which thus becomes the dominant effect for such inversion charge concentrations and for such silicon layer thicknesses. As shown in Fig. 3, the average conduction effective mass decreases as the inversion-charge concentration increases, since the nonprime subband population increases at the expense of the prime-subband population due to size quantization. However, although this mass reduction is more important for the thickest samples, we can see in Fig. 3 that even at high inversion-charge concentrations $m_c$ is still lower in the 5 nm sample, while it tends to coincide in thicker samples. In addition, as for such inversion-charge concentrations, surface-roughness scattering is more important than phonon scattering, the effect of the reduction in the conduction effective mass is dominant over the effect of the increase in the phonon-scattering rate. To illustrate this, Fig. 5 shows electron mobility curves for different silicon layer thicknesses at room temperature, assuming that the conduction effective mass is the same in the two subband ladders. As can be seen, an increase in all the mobility curves is observed, as a consequence of the reduction in the conduction mass, since the electrons in the prime subbands now have the same $m_c$ as the electrons in nonprime subbands. We can also see the effect of the increase in the phonon-scattering rate as $T_w$ decreases, as shown by the mobility reduction at low inversion-charge concentrations where phonon scattering is the main scattering mechanism. However, at high inversion-charge concentrations, and in contrast to the results shown in Fig. 4, all the mobility curves, even the one corresponding to $T_w = 5$ nm, coincide since the conduction effective mass is the same across the entire range of inversion-charge concentrations. This supports the explanation regarding the behavior of the 5 nm mobility curve at high inversion-charge concentrations.

The behavior shown by the mobility curves in Fig. 4 for samples thinner than 10 nm is more marked when Coulomb scattering is considered. Figure 6 shows electron-mobility curves calculated at room temperature taking into account phonon, surface-roughness, and Coulomb scattering. We have assumed that an interface trap concentration of $N_{it} = 5 \times 10^{10}$ cm$^{-2}$ exists in both interfaces.

When Coulomb scattering is considered, it is the main scattering mechanism at low inversion-charge concentrations, rather than phonon scattering. As a consequence, the effect of the reduction in the conduction effective mass becomes more important now, even for lower transverse effec-
while the interface-trap concentration in the gate interface contributes, as predicted in Ref. 9, to explaining the mobility that the greater degradation of the buried interface also contributes, to the closeness of the charge center of the buried interface to

tive fields. This means that the mobility curve corresponding to the thinnest sample ($T_{w} = 5 \text{ nm}$) is greater than the mobility for thicker samples at effective fields much lower than the ones for which this effect is observed when Coulomb scattering is ignored (Fig. 4). Nevertheless, it is interesting to note that the thinner samples also show an increase in the Coulomb-scattering rate due to the interaction with the charged centers of the buried interface (which become closer to the inversion layer electrons as $T_{w}$ is reduced). However, for the interface-trap concentration considered in this figure, this effect is very small and scarcely observable.

We have also studied the role played by the high concentrations of interface-trap density $N_{it}$ in the back interface (buried oxide) (shown by Toriumi et al.) in the degradation of the electron mobility as the thickness of the silicon layer decreases. To do so, we have assumed that the interface-trap concentration in the buried interface is $N_{it} = 5 \times 10^{11} \text{ cm}^{-2}$, while the interface-trap concentration in the gate interface has been taken as the same as before (see the mobility curves in Fig. 7). As expected, a greater separation of mobility curves is observed at low transfer electric fields, indicating that the greater degradation of the buried interface also contributes, as predicted in Ref. 9, to explaining the mobility decrease observed experimentally. Nevertheless, note that while this limitation is a consequence of technological problems (and therefore, expected to be overcome in the near future), the other factor that also contributes to the degradation of the electron mobility as the silicon layer becomes thinner (phonon limitation) is intrinsically linked to the thin SOI device, and is therefore only avoidable at very low temperatures (4.2 K).

In any case, as can be seen in Fig. 7, if the silicon-layer thickness is reduced below 10 nm, the electron mobility at high inversion-charge concentrations improves.

Finally, note that the same mobility behavior as experimentally observed (for silicon-layer thicknesses down to $T_{w} = 10 \text{ nm}$) is obtained in the simulation. Although we have made no explicit comparison between experimental results and simulated ones, we would like to note that both quantitatively and qualitatively, our calculated results are very similar to the mobility data obtained in Ref. 8. The main discrepancies occur at high transverse effective fields, where simulations provide a higher value than the one experimentally found by Choi et al. This discrepancy can be easily bypassed considering in our simulation a different set of values to model the surface-roughness scattering.

**IV. CONCLUSIONS**

In summary, we have shown that there are several facts that affect mobility behavior as the silicon layer thickness is reduced when all the scattering mechanisms are taken into account simultaneously. In addition, we have also demonstrated that their effect depends on the inversion-charge concentration. These facts are: (i) the reduction of the conduction effective mass; (ii) the increase of the phonon-scattering rate; and (iii) the increase in the Coulomb-scattering rate due to the closeness of the charge center of the buried interface to the inversion-layer electrons.

The importance of these effects depends, as mentioned above, both on the silicon-layer thickness and on the inversion-charge concentration. This explains the nontrivial behavior of the electron mobility curve as the silicon-layer thickness is reduced. This behavior can be summarized as follows:

(i) For $T_{w} > 50 \text{ nm}$, the electron mobility does not depend on the silicon thickness.

(ii) For $10 \text{ nm} < T_{w} < 50 \text{ nm}$, the electron mobility decreases as silicon thickness decreases.

(iii) For $T_{w} < 10 \text{ nm}$, the behavior of the electron mobility on the silicon layer thickness depends on the interface trap concentration in the back interface and on the inversion-charge concentration, although a significant improvement is achieved at high inversion-charge concentrations.

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