Role of surface-roughness scattering in double gate silicon-on-insulator inversion layers

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The effect of surface-roughness scattering on electron transport properties in extremely thin double gate silicon-on-insulator inversion layers has been analyzed. It is shown that if the silicon layer is thin enough the presence of two Si–SiO2 interfaces plays a key role, even for a very low transverse effective field, where surface-roughness scattering is already noticeable, contrary to what happens in bulk silicon inversion layers. We have studied the electron transport properties in these devices, solving the Boltzmann transport equation by the Monte Carlo method, and analyzed the influence of the surface-roughness parameters and of the silicon layer thickness. For low transverse effective fields, $\mu_{SR}$ decreases as the silicon layer decreases. However, at higher transverse effective fields, there is a different behavior pattern of $\mu_{SR}$ with $T_w$ since it begins to increase as $T_w$ decreases until a maximum is reached; for lower silicon layer thicknesses, surface-roughness mobility abruptly falls. Finally we have compared the behavior of $\mu_{SR}$ versus $T_w$ for double gate silicon-on-insulator and single gate silicon-on-insulator inversion layers. © 2001 American Institute of Physics.

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I. INTRODUCTION

In a recent article,\textsuperscript{1} we studied the effect of surface-roughness scattering on electron transport properties in extremely thin single gate silicon-on-insulator (SGSOI) inversion layers. The main conclusion of that article was that if the silicon layer is thin enough (thinner than 15 nm) the presence of a second Si–SiO2 interface (the buried interface) plays a very important role. In fact, we showed that the buried interface has a double effect since, on one hand, it modifies the surface-roughness scattering rate due to the gate interface, and on the other, itself provides a non-negligible scattering rate. Thus we demonstrated that it is absolutely necessary to take into account the presence of the second Si–SiO2 interface when studying the electron transport properties in very thin SOI devices.

In order to reach such conclusions we had to modify the usual surface-roughness scattering model used for bulk silicon-inversion layers. In the article referenced above, we showed that if the silicon layer is very thin, the usual surface-roughness scattering model used to simulate bulk silicon inversion layers fails. In particular, it was observed that the bulk model overestimates the effect of surface-roughness scattering due to the gate interface as a consequence of the minimal thickness of the silicon layer. Therefore it was necessary to modify such a model in order to correctly simulate the effect of surface-roughness scattering in very thin SOI inversion layers.

The conclusions and results obtained in our previous work were for SGSOI devices, that is to say, we only had one electric-control terminal. However, as is widely known, there is also a great interest in double gate SOI (DGSOI) devices. In fact, double gate metal–oxide–semiconductor field-effect transistors (DGMOSFETS) are currently considered a serious alternative to standard-bulk MOSFETs to increase the integration capacity of the present silicon technology in the near future. A dual gate silicon-on-insulator (DGSOI) structure consists, basically, of a silicon slab sandwiched between two oxide layers. A metal or polysilicon film is deposited on each oxide. Each one of these films then acts as a gate electrode (front and back gate), which can generate an inversion region near both Si–SiO2 interfaces, if the appropriate bias is applied. Thus we would have two MOSFETs sharing the substrate, source, and drain. The main feature of these structures arises from the concept of volume inversion, introduced by Balestra et al.\textsuperscript{2} some time ago: If the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction takes place between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab (i.e., near the two silicon–oxide interfaces), but throughout the entire silicon film thickness. The device is then said to operate in volume inversion, i.e., the carriers are no longer confined to one interface, but are distributed throughout the entire silicon volume. Several authors have claimed that volume inversion presents a significant number of advantages, such as: (i) an enhancement of the number of minority carriers; (ii) an increase in carrier mobility and velocity due to reduced influence of the scattering associated with oxide and interface charges and surface roughness; (iii) as a consequence of the latter, an increase in drain current and transconductance; (iv) a decrease in low-frequency noise, and (v) a great reduction in hot carrier effects.\textsuperscript{2}

In addition, like other dual gated devices, DGMOSFETS are claimed to be more immune to short channel effects.
structures, see Ref. 4. A detailed discussion on the role of the inversion layer centroid in both the potential wells and the electron distributions for 5-nm silicon-thick SGSOI and DGSOI inversion layers, respectively. In this article, we assume that the same voltage is applied to both gate terminals in the DGSOI device (symmetric operation) and that the inversion charge concentration is the same in both cases ($N_{\text{inv}} = 8 \times 10^{12}$ cm$^{-2}$). To evaluate the inversion charge concentration in the double gate device (symmetric case) we have considered:

$$N_{\text{inv}} = \int_{x_0}^{T_w} n(z) dz \text{(DGSOI)},$$

(1)

where $n(z)$ is the electron distribution, $T_w$ the silicon thickness and $x_0$ the position inside the oxide where the electron concentration vanishes. However, for single gate devices, where only one gate terminal is presented, the whole silicon layer is considered, i.e.,

$N_{\text{inv}} = \int_{x_0}^{T_w} n(z) dz \text{(SGSOI)},$

(2)

(for a detailed discussion, see Ref. 4).

The different electron distributions observed for the two structures might suggest that surface-roughness scattering has a different effect on the transport properties of electrons in each structure. The first difference noted is that the role of both interfaces is fully symmetric in DGSOI devices, while in SGSOI ones the role of the interfaces is quite different, as shown in Ref. 1.

To understand the role of surface-roughness scattering in DGSOI inversion layers, the following two questions should be answered: (i) Could the surface-roughness model developed for very thin SGSOI inversion layers be applied to DGSOI ones and (ii) how does silicon layer thickness affect electron transport properties in very thin DGSOI inversion layers?

In this article we have attempt to provide an answer to these questions. In Sec. II we test the validity of the improved surface-roughness scattering model for DGSOI inversion layers. Then, in Sec. III, a Monte Carlo simulator (developed elsewhere) is used to calculate electron mobility curves. The effect of each interface on electron mobility is comprehensively analyzed. We have also attempted to quantify the influence of the silicon layer thickness and the height of the surface roughness on electron mobility. In this section we compare the effect of surface-roughness scattering on electron mobility in DGSOI inversion layers and SGSOI ones. Finally, the main results and conclusions of our work are summarized in Sec. IV.

It would have been interesting to compare the simulation results with experimental data. However, the lack of adequate samples and mobility data (conveniently characterized) in the literature has prevented us from doing that. In any case, the absence of such a comparison in no way modifies the nature and conclusions of our theoretical study.

II. SURFACE-ROUGHNESS SCATTERING MODEL

Following previous works$^5-7$ and our own, earlier article,$^1$ we have considered that the interface between the silicon and the oxide is an abrupt boundary which randomly varies according to a function $\Delta$ of the coordinate parallel to the surface, $\Delta(\mathbf{r})$. In such conditions, the surface-roughness perturbation Hamiltonian, $H_{\text{sr}}(z, \mathbf{r})$, is given by

$$H_{\text{sr}}(z, \mathbf{r}) = -e(V(z + \Delta(\mathbf{r})) - V(z)),$$

(3)

where $V(z)$ is the unperturbed surface potential and $z$ the coordinate perpendicular to the interface.

As in the case of SGSOI samples, we have two Si–SiO$_2$ interfaces to deal with. As in the previous work, we again assume that the two interfaces are completely uncorrelated and that the superposition principle is valid, that is to say, we consider the surface-roughness scattering by the two interfaces as two different scattering mechanisms.

First, we analyze the effect of one of the interfaces, for example, the one located at $z = 0$. At a given position ($r_0$, $z = 0$) of this interface, we assume a $z$ displacement of the actual interface of $\Delta_1$ nanometers from the ideal interface.
plane located at \(z=0\). The insert of Fig. 2 compares the actual potential at \(r_0\) (dashed line) with the potential we should have obtained for an ideal interface (solid line). The structure considered consists of a \(5\text{-nm}-\text{thick silicon layer sandwiched between two oxide layers 5-nm thick. The same voltage has been applied to both gates and a doping concentration of } D / 3 \text{ has been assumed. Figure 2 shows the perturbation Hamiltonian [expression (3)] for a } z \text{ displacement of } \Delta r_0 = 0.25 \text{ nm. We have also assumed that the oxide thickness is not modified by the interface roughness.}

Let \(\Delta_m\) be the rms value of \(\Delta(r)\), where for a given point \(r\) at the interface, the \(z\) displacement of the interface from an ideal plane is \(\Delta(r)\). To evaluate the perturbation Hamiltonian [Eq. (3)], from our previous work, we assume that

\[
V[z + \Delta(r)] - V(z) = \frac{V(z + \Delta_m) - V(z)}{\Delta_m} \Delta(r). \tag{4}
\]

Therefore the perturbation Hamiltonian due to surface-roughness scattering is now

\[
H_{\text{SR}}(z, r) = -\frac{e \Delta(r) \Delta V_m(z)}{\Delta_m}, \tag{5}
\]

where

\[
\Delta V_m(z) = V(z + \Delta_m) - V(z). \tag{6}
\]

Figure 2 compares the perturbation Hamiltonian given by expression (5) (bold circles) with the exact perturbation Hamiltonian [expression (3)] for a given point at the interface \(r_0\) (bold squares), where \(\Delta(r_0) = 0.25 \text{ nm. } \Delta_m\) is considered to be 0.5 nm. The coincidence of the two curves proves that this model also accurately reproduces the perturbation Hamiltonian in the DGSOI case.

Using this approximation for the perturbation Hamiltonian, the matrix element for surface-roughness scattering in the Born approximation is finally given as

\[
|M_{\mu\nu}(q)|^2 = |\langle \nu, k | H_{\text{SR}} | \mu, k' \rangle |^2
= e^2 \int \psi_{\mu}(z) \frac{\Delta V_m(z)}{\Delta_m} \Psi_{\mu}(z) dz \| \Delta(q) \|^2,
\]

where \(\mathbf{k}'\) is the electron wave vector before the scattering, \(\mathbf{k}\) the electron wave vector after the scattering, \(q = \mathbf{k} - \mathbf{k}'\), \(e\) is the electron charge, \(\psi_{\mu}(z)\) the envelope function in the \(\mu\)th subband, and \(\Delta(q)\) is the Fourier transform of \(\Delta(r)\). Therefore to evaluate this matrix element we have to previously evaluate \(\Delta V_m(z)\) according to Eq. (5).

Following the work of Goodnick et al., an exponential model for \(|\Delta(q)|^2\),

\[
|\Delta(q)|^2 = \frac{\pi \Delta_m^2 L^2}{(1 + q^2 L^2/2)^{3/2}} \tag{8}
\]

has been assumed, where \(L\) is the autocovariance length of the roughness fluctuations.

The surface-roughness scattering rate (including screening effect) for an electron with wave vector \(\mathbf{k}\) in the \(\mu\) subband and final state in the \(\nu\) subband is finally given by

\[
\frac{1}{\tau_{\text{SR}}(k)} = \frac{m_e e^2}{2\hbar^2} \left| \int_0^{2\pi} \frac{d\theta}{\epsilon(q)(1 + L^2 q^2/2)^{3/2}} \right|
\]

\[
\times \int_0^{q^2 = 2k^2(1 - \cos \theta)} F(q) d\theta, \tag{9}
\]

where \(\epsilon(q)\) is given by

\[
\epsilon(q) = 1 + \frac{e^2 m_d}{2 \epsilon q \pi \hbar^2} F(q) \tag{10}
\]

and

\[
F(q) = \sum_m \int dz \int dz' \left| \psi_m(z) \right|^2 \left| \psi_m(z') \right|^2 e^{i q(z - z')}. \tag{12}
\]

The model given by expressions (9)–(12) can be extended naturally in order to take into account the effect of the roughness of the second interface, that is to say; the one located at \(z = T_w\). Following the steps given above, it is possible to evaluate the perturbation Hamiltonian arising from a displacement of this interface from an ideal plane. As expected, the perturbation Hamiltonians for the two interfaces are fully symmetric. In addition, as the electron distribution is also symmetric (Fig. 1), both interfaces provide the same matrix element, and thus the same scattering rate.

**III. ELECTRON MOBILITY CALCULATION**

Once we have evaluated the scattering matrix elements due to the roughness of both interfaces, we can calculate the electron mobility in these ultrathin inversion layers. To do so, we used a one-electron Monte Carlo simulator that had been developed previously.
Electron quantization in the ultrathin inversion layer has been taken into account by self-consistently solving the Poisson and Schrödinger equations. Only phonon and surface-roughness scattering have been taken into account in this work. For the phonon scattering, bulklike scattering models were taken into consideration. We considered acoustic deformation potential scattering and intervalley phonon events (both between equivalent and nonequivalent valleys). The coupling constants for the intervalley phonons and the acoustic deformation potential were the same as in bulk silicon inversion layers.\(^1\) The phonon-scattering rates for inversion layers were deduced by using Price’s formulation (a detailed description of this simulation can be found elsewhere).\(^1,9,10\)

As mentioned before, in the present work we attempt to show the effect of surface roughness scattering on electron mobility in ultrathin double gate silicon inversion layers. To do so, we calculated electron mobility curves for different silicon layer thicknesses and different surface-roughness heights at room temperature, using the Monte Carlo simulator described above.

Figure 3 shows the electron mobility curves as a function of the transverse effective field, defined for symmetric DGSOI inversion layers as

\[
E_{\text{Eff}} = \frac{\int_{z_0}^{T_w/2} n(z) E(z) dz}{\int_{z_0}^{T_w/2} n(z) dz},
\]

where \(E(z)\) is the local transverse electric field.\(^14,15\) The same structure as described in Sec. II has been assumed. Different values of the silicon thickness, \(T_w\), were considered. In addition, for each \(T_w\) value, different sets of surface-roughness parameters were assumed: (solid line): No surface-roughness scattering, i.e., the two interfaces were assumed ideal, and therefore the only scattering mechanism is phonon scattering; (solid squares): \(\Delta_1 = \Delta_2 = 0.25\) nm, \(L_1 = L_2 = 1.5\) nm.

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The first fact that to note in Fig. 3 is that mobility curves fall significantly as a consequence of the contribution of surface roughness mobility, mainly at high transverse effective fields. In addition, the importance of the surface-roughness scattering increases as the silicon layer thickness decreases. For the thinnest samples (\(T_w = 20\) and 10 nm) the surface-roughness scattering only affects electron mobility at high transverse effective fields, even for the roughest sample. However, for the thinnest samples, the effect of surface-roughness scattering is noticeable even at very low transverse effective fields. Therefore as the silicon layer decreases, the importance of the surface-roughness effect grows. This is due to the fact that for the thinnest samples, the confinement of the electrons near the Si–SiO\(_2\) interfaces is due to the thinness of the silicon layer.

Another noticeable feature that can be observed in Fig. 3 is the effect on the phonon-limited mobility (solid curves) as a consequence of the silicon layer thickness. Some details of the effect of silicon layer thickness on phonon scattering in SGSOI inversion layers have already been given in Ref. 1 and 16 and references therein. The behavior observed in the phonon-limited mobility (solid line) is a consequence of the increase in the phonon scattering rate due to the greater confinement of the electrons as the silicon film thickness shrinks,\(^17,18\) since the less localized the electrons are in the wave vector space, the higher the number of phonons that can assist carrier transitions.\(^12,13,19,20\) A more comprehensive study of the role of phonon-limited mobility in DSGOI inversion layers is being developed.

In a previous work, Shoji et al.\(^14,15\) showed an important enhancement of the phonon-limited mobility around \(T_w = 3\) nm. Nevertheless, as can be observed in Figs. 3 and 4, when surface-roughness scattering is considered this mobility enhancement fully disappears.

As the scope of the present work is the study of surface-roughness scattering, we thought it useful to isolate the contribution of this scattering mechanism. To do so, we applied the Matthiessen rule to the mobility data of Fig. 3:

\[
\frac{1}{\mu_{\text{SR}}} = \frac{1}{\mu_{\text{total}}} - \frac{1}{\mu_{\text{phonon}}},
\]

where \(\mu_{\text{SR}}\) is the mobility due to surface-roughness scattering alone, \(\mu_{\text{phonon}}\) is the mobility due to phonon scattering alone, and \(\mu_{\text{total}}\) is the mobility due to both surface-roughness and phonon scattering. Although the application of Matthiessen’s rule to the case of high temperatures and high inversion charge concentrations (the case dealt with here) is questionable and can lead to inaccurate quantitative results, it is interesting to analyze the mobility due to surface roughness alone, since this sheds some light on the effect of this scattering mechanism.

Figure 4 shows the result of applying Matthiessen’s rule to the mobility curves of Fig. 3, from which, the following conclusions can be drawn.
(a) For the same silicon layer thickness, $\mu_{\text{SR}}$ decreases as the transverse effective field increases, as expected. The high transverse electric fields push the electrons towards the interfaces, where the surface-roughness perturbation Hamiltonian is bigger, as seen in Fig. 2. This makes the surface-roughness scattering rate increase.

(b) However, the $\mu_{\text{SR}}$ decrease is steeper for the thickest samples. This means that at low transverse effective fields, the thinner the silicon layer, the stronger the scattering rate and therefore the lower the electron mobility. However, at high transverse effective fields, the trend is reversed, and thicker samples have lower surface-roughness mobility.

In order to show the dependence of $\mu_{\text{SR}}$ on the silicon layer thickness more clearly, Fig. 5 illustrates the evolution of surface-roughness mobility with the silicon layer thickness for different values of the transverse effective field. In this figure we see that at low transverse effective fields the surface-roughness mobility decreases as the silicon layer decreases. However, at high inversion charge concentrations, a different behavior is observed. As the silicon layer is reduced, $\mu_{\text{SR}}$ increases until a maximum value in the range $10^{-5}$ nm depending on the $E_{\text{EFF}}$ value is reached. This is the region where the interaction between the two channels makes the electrons spread along the silicon layer, thus reducing the surface-roughness scattering rate. Finally, for lower $T_w$ values the surface-roughness mobility abruptly decreases, due to the high geometrical confinement of the electrons.

In the case of SGSOI inversion layers, we saw that the role played by the buried interface was quite different to the one played by the gate interface. However, as stated above, the role played by both interfaces in DGSOI inversion layers is fully symmetric. To check this we simulated mobility curves, assuming that: (i) the two interfaces are ideal (i.e., there is not surface-roughness scattering at all) (Fig. 6, dotted line), (ii) one of the two interfaces is ideal (Fig. 6, dashed line), and (iii) the two interfaces are affected by surface roughness (Fig. 6 solid line). A silicon layer thickness of 3 nm was considered, with surface-roughness parameters of: $\Delta = 0.5$ nm, $L = 1.5$ nm. If we apply Matthiessen's rule to mobility curves of Fig. 6 it can be observed that $\mu_{\text{SR}}$ when
only one interface is considered to be rough (dashed line) is exactly twice $\mu_{SR}$ when both interfaces are affected by roughness.

Finally, we also compared the surface-roughness mobility in DGSOI and SGSOI devices. The structure we have considered for the SGSOI inversion layer consists of a very low doped (100)-silicon film sandwiched between two oxide layers. The gate-oxide thickness was taken as 5 nm, while the buried oxide was considered to be 80-nm thick. A silicon substrate was assumed under the buried oxide. A $P^+\text{POLY}$ gate was employed. Figure 7 compares $\mu_{SR}$ for both devices as a function of the silicon layer thickness for different values of the transverse effective field. In this figure, the following three regions can be observed.

(i) There exists a region for large $T_w$ values, where no interaction between the two channels is produced, and the mobility curves for DGSOI and SGSOI coincide. In addition, these mobility values are very similar to the values obtained for bulk silicon inversion layers. (In fact the trend of these curves for larger $T_w$ values coincides with the bulk value, as shown in Fig. 7.) This coincidence in mobility for DGSOI and SGSOI mobility curves for such silicon thicknesses is due to the identical electronic structures of the inversion layers for values of $T_w$.14,15

(ii) In the second region (intermediate values of $T_w$), electron mobility of DGSOI inversion layers is greater than that corresponding to SGSOI inversion layers. This is the region where the volume inversion occurs. This region is between $3 \text{ nm} < T_w < 15 \text{ nm}$. In this region, surface-roughness scattering is reduced as a consequence of the spread of electrons throughout the silicon volume (volume inversion). To clarify this we calculated the perturbation Hamiltonian due to a displacement of one of the interfaces of $\Delta_m=0.25 \text{ nm}$, and the scattering matrix element $|M_{\mu\nu}(q)|^2$, due to this perturbation Hamiltonian. A DGSOI inversion layer with $T_w=5 \text{ nm}$ was considered. These results were compared to the ones obtained for the same displacement of one of the two interfaces in a SGSOI inversion layer of the same thickness (Fig. 8). It can be seen that the perturbation Hamiltonian and therefore the scattering matrix element are lower in the case of a DGSOI structure. Therefore we can conclude that in this region surface-roughness mobility is also improved as a consequence of volume inversion.

(iii) Finally, for $T_w<3 \text{ nm}$, the electron mobility curves of both structures coincide again. In this region, controlled by geometric effects, mobility decreases abruptly.

IV. SUMMARY

The effect of surface-roughness scattering on electron transport properties in extremely thin double gate silicon-on-insulator inversion layers has been analyzed. It is shown that if the silicon layer is thin enough (thinner than 10 nm), the presence of two Si–SiO$_2$ interfaces plays a very important role, even for a very low transverse effective field, where surface-roughness scattering is already noticeable, on the contrary to what happens in bulk silicon inversion layers. We have shown that the surface-roughness scattering model developed for SGSOI devices is also applicable to DGSOI devices. Thus the proposed model allows us to evaluate the surface-roughness scattering rate due to both interfaces, which as is shown, play a symmetric role. After evaluating the scattering rates, the electron mobility was calculated by the Monte Carlo method. As our goal was to study the effect of surface roughness, only phonon and surface-roughness scattering mechanisms were taken into account in our simulation. The influence of surface-roughness parameters and of silicon layer thickness was analyzed. For low transverse eff-
fective fields we found that $\mu_{\text{SR}}$ decreases as the silicon layer decreases. However, at higher transverse effective fields, there is a different behavior pattern of $\mu_{\text{SR}}$ with $T_w$, since it begins to increase as $T_w$ decreases until a maximum is reached; for lower silicon layer thicknesses, surface-roughness mobility abruptly falls. Finally we compared the behavior of $\mu_{\text{SR}}$ versus $T_w$ for DGSOI and SGSOI inversion layers, revealing the existence of three regions:

1. For large $T_w$ values, mobility for DGSOI and SGSOI coincides;
2. In the intermediate range of $T_w$ values, $\mu_{\text{DGSOI}} > \mu_{\text{SGSOI}}$, and finally,
3. For very thin layers, both mobility curves coincide again.

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