Electron mobility in double gate silicon on insulator transistors: Symmetric-gate versus asymmetric-gate configuration

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We have studied electron mobility behavior in asymmetric double-gate silicon on insulator (DGSOI) inversion layers, and compared it to the mobility in symmetric double-gate silicon on insulator devices, where volume inversion has previously been shown to play a very important role, being responsible for the enhancement of the electron mobility. Poisson’s and Schroedinger’s equations have been self-consistently solved in these structures to study and compare the distribution of the electrons. We show that the lack of symmetry in the asymmetric DGSOI structure produces the loss of the volume inversion effect. In addition, we show that as the silicon thickness is reduced the conduction effective mass of electrons in asymmetric devices is lower than that in the symmetric case, but that the greater confinement of electrons in the former case produces a stronger increase in the phonon scattering rate, and in the surface roughness scattering rate. We have solved the Boltzmann transport equation by the Monte Carlo method, and have evaluated the electron mobility. The electron mobility curves in asymmetric DGSOI devices are shown to be considerably below the mobility curves corresponding to symmetric devices, in the whole range of silicon thicknesses. The difference is greater in the range 5–25 nm, where electron mobility in symmetric DGSOI inversion layers is greatly improved by the volume inversion effect. We show that mobility in symmetric devices could be 2.5 times greater than that for their asymmetric counterparts. © 2003 American Institute of Physics. [DOI: 10.1063/1.1615706]

I. INTRODUCTION

Double-gate metal–oxide–semiconductor-field-effect-transistors (DGMOSFETs) are currently considered a serious alternative to standard-bulk MOSFETs to increase the integration capacity of present-day silicon technology in the near future, especially beyond the 10 nm barrier.1,2 A double-gate-silicon-on-insulator (DGSOI) structure consists, basically, of a silicon slab sandwiched between two oxide layers. A metal or polysilicon film is deposited on each oxide (Fig. 1). Each of these films then acts as a gate electrode (front and back gate), which is capable of generating an inversion region near the two Si–SiO2 interfaces, if the appropriate bias is applied. If the Si thickness is reduced enough, the whole silicon film is depleted and the inversion layer is formed throughout the entire silicon film thickness. The device is then said to operate in volume inversion, i.e., the carriers are distributed throughout the entire silicon volume.3,4

There are two main types of DGMOSFETs (Fig. 1): (1) a symmetric type with both gates of identical work functions so that the two surface channels turn on at the same gate voltage [Fig. 1(a)] and (2) an asymmetric type with different work functions for the gates and in which only one channel turns on at the threshold voltage [Fig. 1(b)].5,6 The threshold voltage of the symmetric device is determined by the work function of the gate material, and it is negligibly dependent on the silicon thickness, the silicon doping concentration or the oxide thickness.7 Figure 2 shows the threshold voltage of a symmetric DGSOI structure using p+-polysilicon gates (dashed line) and n+-polysilicon gates (solid line) as a function of the silicon thickness $t_{\text{Si}}$. Both oxide thicknesses were considered to be $t_{\text{ox}}=1$ nm, the silicon doping was taken as $N_A=10^{15}$ cm$^{-3}$, and the doping of the polysilicon gate $N_{D,poly}=N_{A,poly}=1\times10^{20}$ cm$^{-3}$. To calculate these curves we have self consistently solved the Poisson and Schroedinger equations in the DGSOI structure. The threshold voltage $V_{\text{th}}$ has been taken as the gate voltage necessary to induce an inversion charge concentration of $N_{\text{inv}}=10^{11}$ cm$^{-2}$ in the silicon layer. As already known,6 the threshold voltage values obtained with the symmetric structure are, depending on the type of doping of the gate polys, too high ($\sim1$ V for $p^+$-polysilicon gates) or too low ($\sim0.1$ V for $n^+$-polysilicon gates), and in any case, inadequate for the state-of-the-art technology. Therefore, it is necessary to look for different gate materials if we want these symmetric DGSOI devices to have an appropriate threshold voltage to be used in low-power and high speed applications. However, Suzuki and Sugii6 proved that it is still possible to control the threshold voltage of a DGSOI device with polysilicon gates if an asymmetric $n^+-p^+$ structure is used. Figure 2 (solid line) shows the voltage threshold for an asymmetric $n^+-p^+$ DGSOI device as a function of the silicon thickness. As observed, the interaction between the two gates allows the control of the threshold voltage in this structure to suitable values for the state-of-the-art applications. Therefore, from this point of view, it seems that an asymmetric configuration could prove superior to a symmetric one. Other studies have

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also highlighted this superiority of asymmetric devices.

(i) Suzuki and Sugii used a charge sheet approximation to develop an analytic model for asymmetric DGMOSFETs. They showed that it is possible to design asymmetric DGSOI devices with sub-0.1 \( \mu \text{m} \) gate length with an appropriate threshold voltage and an ideal subthreshold swing.

(ii) Kim and Fossum have presented numerical device-simulation results, supplemented by analytic characterizations, to argue that asymmetric DGMOSFETs, utilizing \( n^+ \) and \( p^+ \) polysilicon gates, can be superior to symmetric-gate counterparts for several reasons, only one of which is its previously noted threshold-voltage control. The threshold voltage in DGSOI devices has been shown to be more easily controlled via asymmetric gates of \( n^+ \) and \( p^+ \) polysilicon which, however, would seem to undermine the current drive because the resulting device has only one predominant channel. On the contrary, it has been shown by MEDICI simulations that the gate–gate coupling in the asymmetric DGMOSFET is more beneficial than in the symmetric counterpart, resulting in the superiority of the former device for more reasons than just the threshold-voltage control.

(iii) Taur analytically solves a one-dimensional (1D) Poisson equation with only the inversion charge term for an undoped DGMOSFET. This solution is applied to both symmetric and asymmetric DGMOSFETs to obtain closed forms of band bending and inversion charge as a function of gate voltage and silicon thickness. However quantum effects are ignored, and therefore the inversion charge distribution cannot be adequately described since, as the silicon and oxide thicknesses are reduced, quantum size effects become very important in these devices.

The previously mentioned studies provide important results based on the electrostatic gate–gate coupling in both devices. From these results, it is concluded that asymmetric double gate devices could be superior to their symmetric counterparts based on a higher drive current at lower applied voltages. However, these results were obtained assuming that electron mobility in the two devices is similar. Our Monte Carlo results show that electron mobility in symmetric DG devices could be very different from that in asymmetric DG devices.

In previous works, we studied the electron mobility in a symmetric DGSOI device as a function of the transverse effective field and silicon layer thickness. The contributions of the main scattering mechanisms (phonon scattering, surface roughness scattering due to both Si–SiO\(_2\) interfaces, and Coulomb interaction with the interface traps of both interfaces) were taken into account and carefully analyzed. We demonstrated that the contribution of surface scattering mechanisms is by no means negligible; on the contrary, it plays a very important role which must be taken into account when calculating the mobility in these structures. The electron mobility in symmetric DGSOI devices as \( T_e \) decreases is compared with the mobility in single-gate silicon-on-insulator structures and in bulk silicon inversion layers: (i) when only phonon scattering is considered; (ii) when the effect of surface-roughness scattering is taken into account; and (iii) when the contribution of Coulomb interaction with charges trapped at both interfaces is taken into consideration.
(in addition to phonon and surface roughness scattering). From this comparison we determined (in the three cases above) the existence of the following three regions: (i) A first region for thick silicon layers ($T_w > 20–30$ nm), where mobility for both structures tends to coincide, approaching the bulk value. (ii) As $T_w$ decreases we show that volume inversion modifies the electron transport properties by reducing the effect of all scattering mechanisms. Accordingly, the electron mobility in symmetric DGSOI inversion layers increases by an important factor which depends on the silicon thickness and the transverse effective field. (iii) Finally, for very small thicknesses, the limitations to electron transport are due to geometrical effects, and therefore the two mobility curves, which again coincide, fall abruptly. We show the existence of a range of thicknesses of a silicon layer (between 5 and $20$ nm) in which electron mobility is improved by 25% or more, due to volume inversion. Therefore, volume inversion and the symmetry of the device play an important role in the electron mobility in these symmetric DGSOI devices as the silicon thickness is reduced below 20 nm. Of course, symmetry is lost in asymmetric DGSOI devices, and the question which arises here is whether this fact also means the loss of the volume inversion effect and, as a consequence, of their advantages from the mobility viewpoint. As mentioned above, it seems from electrostatic studies, that asymmetric DGSOI devices could show a better behavior than their symmetric DGSOI counterparts. However, it is then necessary to answer the following: How does electron mobility in asymmetric DGSOI devices behave compared to that in symmetric DGSOI devices? Until an answer is provided, the choice of symmetric or asymmetric gates is still an open question.$^{2,10}$

To shed some light on the above question, we have made an in-depth study of electron mobility behavior in asymmetric DGSOI devices, and have compared it with the mobility in their symmetric counterparts. To do so, we have followed a procedure similar to that adopted in Ref. 4 to study symmetric DGSOI devices. Thus, we used a one-electron Monte Carlo method to study the stationary electron transport properties in asymmetric DGSOI inversion layers, focusing our attention on the evaluation of the stationary drift velocity and the low-field mobility at room temperature. Electron quantization in the inversion layer was appropriately taken into account, and Poisson’s and Schrödinger’s equations were self-consistently solved assuming a simple nonparabolic band model for the silicon. Once the electron distribution in the silicon layer had been determined, the Boltzmann transport equation was solved by the Monte Carlo method, simultaneously taking into account phonon and surface-roughness scattering. As demonstrated previously,$^{4,11–14}$ the presence of two close silicon-oxide interfaces in both single and DGSOI MOSFETs produces a significant difference with respect to their standard-bulk counterparts. Therefore, we had to develop improved models capable of taking into account the effect of the roughness of both interfaces$^{11,12}$ on the total scattering rate, and models to calculate the Coulomb scattering rate in ultrathin SOI structures,$^{14}$ which have been shown to be different from the models used for conventional silicon bulk inversion layers. We considered asymmetric n-channel DGSOI MOSFETs with different values of silicon thickness. The distribution of the electrons was evaluated by self-consistently solving the Poisson and Schrödinger equations, and compared to that obtained for symmetric devices with the same value of electron concentration. The role of volume inversion in asymmetric DGSOI devices is investigated in Sec. II. Electron mobility curves for asymmetric DGSOI MOSFETs are evaluated in Sec. III using a one-electron Monte Carlo simulator to solve the Boltzmann transport equation for different values of the silicon thickness. The evolution of the electron mobility with the silicon thickness in asymmetric devices is compared with that for symmetric devices. Finally, the main conclusions of this work are drawn in Sec. IV.

II. ELECTRON DISTRIBUTION, POISSON, AND SCHROEDINGER SOLUTION

The structure we have considered is shown in Fig. 1(b). It consists of a lightly doped ($N_A = 1 \times 10^{15}$ cm$^{-3}$) silicon layer sandwiched between two oxide layers 1 nm thick ($t_{ox} = 1$ nm). Two polysilicon gates were assumed as control electrodes. The front upper gate was $n^+$ doped ($N_{D-polys} = 1 \times 10^{20}$ cm$^{-3}$) while the back lower gate was $p^+$ doped ($N_{A-polys} = 1 \times 10^{20}$ cm$^{-3}$). The same gate voltage was applied simultaneously to both gates ($V_{G1} = V_{G2} = V_G$). Different silicon layer thicknesses, ranging from $T_w = 1.5$ nm to $T_w = 50.0$ nm were considered. For a better understanding of the behavior of these asymmetric DGSOI devices, we compared their properties to those of symmetric DGSOI devices. Symmetric DGSOI devices [Fig. 1(a)] are obtained from asymmetric devices by changing the doping of the back lower poly gate from $p^+$ to $n^+$. Quantum size effects are known to become very important in these devices (since carriers are confined by the silicon thickness which is comparable to the De Broglie wavelength of the carriers) and therefore, the self-consistent solution of Poisson’s and Schrödinger’s equations is required to evaluate the spatial distribution of the electrons in the silicon layer (for details see Ref. 4).

Figure 3 shows the electron distribution, $n(z)$, throughout the silicon layer in symmetric and asymmetric DGSOI inversion layers for a silicon thickness of $T_w = 5.0$ nm, as a function of the inversion charge concentration, $N_{inv}$, defined here as

$$N_{inv} = \int_{0}^{T_w} n(z)dz,$$

(1)

where $n(z)$ is the electron distribution. Figure 4 shows the potential well for the same structures.

As can be observed in Fig. 3 (and detailed in Ref. 4), in the symmetric case volume inversion is achieved for low inversion charge concentrations, that is to say, carriers are distributed throughout the entire silicon slab. As the inversion charge concentration increases, two channels start to be formed near each Si/SiO$_2$ interface, and the situation is similar to that of two channels connected in parallel. As shown in Ref. 4, having only one channel occupying the entire silicon slab (i.e., the volume inversion condition) or having two al-
most independent channels isolated by a depletion region depends on the degree of interaction between the two potential wells originated by the polarization near each Si–SiO₂, i.e., on the silicon thickness and on the inversion charge concentration value: for high values of \( T_w \) (\( T_w > 30 \) nm), volume inversion is achieved only for extremely low \( N_{\text{inv}} \), but as the silicon thickness is reduced (\( T_w < 15 \) nm) important values of \( N_{\text{inv}} \) can be achieved while maintaining the condition of volume inversion. Indeed, for an ultrathin silicon thickness (\( T_w < 5 \) nm) volume inversion is achieved in the whole range of inversion charge concentration. As we have shown, this volume inversion effect greatly influences the electron transport properties in these devices, as detailed in Ref. 4.

On the other hand, the picture is completely different in asymmetric-gate devices. As shown in Figs. 3 and 4, only one channel is formed near the \( n^+ \) gate, even for very low inversion charge concentrations. Only when the bias potential (which is simultaneously applied to both gates) becomes high enough (greater than 1.1 V) does a second channel start to form at the \( p^+ \)-gate Si–SiO₂ interface, but with an electron concentration much lower than that of the \( n^+ \) gate. Therefore, it might be thought that the volume inversion condition is not achieved in asymmetric devices for silicon layer thicknesses greater than 5 nm.

However, one might also wonder what happens when the silicon layer thickness is comparable to, or even less than that of a typical inversion layer, i.e., when the silicon thickness, \( T_w \), is smaller than 3 nm. Figure 5 shows the potential well and the electron distribution for the structures mentioned above (the solid line corresponds to symmetric device and the dashed line to the asymmetric device). The silicon thickness was taken as 2 nm, and the inversion charge concentration was taken as \( N_{\text{inv}} = 1 \times 10^{12} \text{ cm}^{-2} \). As observed, for this value of the silicon thickness, electrons also populate the entire silicon slab in the asymmetric case, although the charge distribution drifts slightly towards the \( n^+ \) gate. Therefore, one might consider that volume inversion is also achieved in the asymmetric case for these extremely thin silicon layers. However, we will see in the next section that the drift of the electron distribution towards the \( n^+ \) gate produces a higher surface-roughness scattering rate in the asymmetric case.

In summary, volume inversion is lost in asymmetric-gate devices for \( 5 \text{ nm} < T_w < 20 \text{ nm} \), although is kept for \( T_w < 3 \text{ nm} \). As detailed in Ref. 4, volume inversion is responsible for an important enhancement of the electron mobility in symmetric-gate DGSOI devices for \( T_w \) in the range 5–20 nm. As we have just seen, there is no volume inversion in asymmetric devices for 5 nm < \( T_w < 20 \) nm. This fact determines the electron transport properties of asymmetric DGSOI devices, compared to their symmetric counterparts.

In the analysis of the behavior of electron mobility in both single-gate SOI inversion layers and symmetric
double gate SOI inversion layers, we saw that two important and opposite effects appear on electron mobility as the silicon thickness is reduced:

1. On the one hand, the subband modulation effect, or equivalently a decrease in the average conduction effective mass.
2. On the other hand, an increase in the phonon scattering rate.

A. Subband-modulation effect

The first effect, the subband modulation effect, is related to the redistribution of the carriers among the different electronic subbands originated by the size quantization. The self-consistent solution of the Poisson and Schrödinger equations in an SOI inversion layer shows that the separation between the energy levels of the two subband ladders produced by the splitting of the degeneration of the silicon valleys, as a consequence of size quantization, increases as the thickness of the silicon layer is reduced. An important consequence of this fact is that the population of nonprimed subbands increases at the expense of the prime subband population as the silicon layer thickness is reduced, as shown in Fig. 6, where the evolution of the subband population is shown as a function of the silicon thickness. Note that the population of nonprimed subbands is higher in the asymmetric case than in the symmetric case for the same $T_w$ value. This is a consequence of the greater depth of the potential well, which produces a higher size quantization effect, and therefore a greater splitting between nonprimed and primed subbands in the asymmetric case.

B. Phonon scattering increase

Another important effect that appears in SOI inversion layers with decreasing thickness of the silicon layer is an increase in the phonon-scattering rate. Due to the presence of the second Si–SiO$_2$ interface, uncertainty concerning the location of the electrons in the direction perpendicular to the interface is lower in SOI samples than in bulk samples. By the uncertainty principle, there is a wider distribution of the electron’s momentum perpendicular to the interface, which produces a greater phonon-scattering rate. Numerically, this effect is reflected in the following form factor:

$$I_{\mu\nu} = \int_{-\infty}^{\infty} |\psi_{\mu}(z)|^2 |\psi_{\nu}(z)|^2 dz,$$

The redistribution of the population has a direct consequence on the electron transport properties since the conduction effective mass of electrons in non-primed subbands is much lower than that in primed subbands. As a consequence, in both cases, symmetric and asymmetric, a reduction in the conduction effective mass is produced as the silicon thickness decreases, as shown in Fig. 7. A lower conduction effective mass contributes to a decrease in the electron mobility. In addition, the conduction effective mass in asymmetric devices is lower than in symmetric devices, which is in accordance with the argument of the above paragraph. Note, however, that conduction effective masses for symmetric and asymmetric devices tend to coincide for $T_w < 3$ nm.
which multiplies the phonon scattering rates, \( 16 \) where \( \psi_n(z) \) is the envelope of the electron wave function in the direction perpendicular to the interface in the \( n \)th subband.

However, in symmetric DGSOI devices, we have shown that volume inversion means that in the range 5–20 nm, the phonon scattering rate decreases instead of increasing.4 Figure 8 shows the above form factor for the ground subband (\( m^* = n^* \)) for symmetric and asymmetric devices. The curves corresponding to the symmetric DGSOI inversion layers reveal that for thinner samples the form factor is very large due to the geometrical confinement of electrons in a very narrow space. As the silicon slab thickness increases, the form factor is quickly reduced, until a minimum is reached in the region between 5 and 15 nm. Then, it increases to approach, for thick samples (\( T_w > 20 \) nm), the value presented in bulk silicon inversion layers. As can be seen in the figure, in the range \( T_w = 5–15 \) nm the form factor for symmetric DGSOI is lower than that corresponding to bulk inversion layers (\( T_w \rightarrow \infty \)). Consequently, in this range the phonon scattering rate in DGSOI inversion layer decreases, instead of increasing as expected. This is an important result, a direct consequence of the volume inversion effect. Thus, we can show that there exists a range of silicon layer thicknesses where electron mobility for symmetric DGSOI inversion layers is greater than that for bulk inversion layers.4 Direct mobility measurements have recently demonstrated this fact.18

We have seen in the previous section that the lack of symmetry in asymmetric gate devices produces the loss of volume inversion for silicon thickness greater than 3 nm. (This is the range where the decrease in phonon scattering rate is produced in symmetric devices). A consequence of the loss of volume inversion in this range of \( T_w \) values is that the form factor [Eq. (2)] monotonously decreases as the silicon thickness decreases in asymmetric devices, as shown in Fig. 8. This means that the phonon scattering rate for asymmetric devices is higher than that for their symmetric counterparts, and higher than that for bulk silicon inversion layers, as expected. Note, however, that for \( T_w < 3 \) nm, symmetric and asymmetric devices almost show the same value of the form factor.

In summary, the electrons in asymmetric DGSOI devices with \( 5 \) nm < \( T_w < 20 \) nm show a smaller conduction effective mass and a higher phonon scattering rate, compared to symmetric devices. The two effects have an opposite influence on electron mobility. Thus, \( a \ priori \), nothing can be said about the mobility behavior until the Boltzmann transport equation is solved. On the other hand, for \( T_w < 3 \) nm electrons in asymmetric and symmetric devices show similar values for the average conduction effective mass and the phonon scattering rate.

### III. SYMMETRIC VERSUS ASYMMETRIC DEVICES: A MOBILITY VIEWPOINT

To study electron mobility behavior in asymmetric DGSOI inversion layers, we used a one-electron Monte Carlo simulator, developed and described elsewhere.4,12,13
In the discussion following Figs. 7 and 8, and from the comparison of the two kinds of devices (symmetric and asymmetric), we drew the following conclusions for devices with \( T_w > 5 \) nm.

(i) As the silicon thickness is reduced, the conduction effective mass of electrons in the asymmetric case is lower than that in the symmetric case (Fig. 7). This would contribute to an increase in the electron mobility in the former devices.

(ii) The greater confinement of electrons in the asymmetric case, produced by the deeper potential well in the \( n^+ \)-gate side, produces an increase in the phonon scattering rate. This would contribute to a decrease in the mobility in the asymmetric case.

Therefore, taking both facts into account, a priori, it is not possible to foresee the behavior of the mobility until a solution of the Boltzmann transport equation is provided.

Figure 9 shows the evolution of the electron mobility versus the silicon thickness for two values of the inversion charge concentration [as defined in Expression (1)] (symmetric-gate devices in solid line and asymmetric-gate devices in dashed line). Only phonon scattering has been taken into account in this simulation. The first result obtained from these figures is that the lack of symmetry in the asymmetric devices results in a lower degree of mobility than in their symmetric counterparts, for silicon layer thicknesses in the range \( 5 \text{ nm} < T_w < 20 \text{ nm} \). Therefore, the second of the effects (increase in the phonon scattering) rate is dominant on the lower conduction effective mass. However, for the thinnest samples (\( T_w < 3 \text{ nm} \)) the two curves (symmetric and asymmetric) tend to behave similarly (although the mobility peak around 2 nm is lower in the asymmetric-gate case). (For a detailed discussion of phonon-limited mobility behavior in ultrathin SOI devices see Refs. 4, 13, and 19). Therefore, we can conclude that in the range \( 5 \text{ nm} < T_w < 20 \text{ nm} \), phonon limited mobility in asymmetric-gate devices is considerably below the phonon-limited mobility curves due to the lack of volume inversion, and that for \( T_w < 3 \text{ nm} \) phonon-limited mobility behaves similarly in both devices, due to the geometrical confinement of carriers in a very narrow space in both devices.

Phonon scattering is not the only scattering mechanism which affects carriers transport in these devices. In Ref. 4, we show that interface scattering mechanisms are by no means negligible. Surface roughness scattering due to the deviation of the Si/SiO2 interface from an ideal plane is also an important scattering mechanism, mainly for ultrathin silicon layers.\(^{11,12}\) One may also think that the contribution of Coulomb scattering could be taken into account. However, in a DGMOSFET, short channel effects are controlled by device geometry,\(^{20,21}\) as compared to bulk FET where short channel effects are controlled by doping (channel doping and/or halo doping). Therefore, in principle, the channel of a DGMOSFET can be undoped, which allows better carrier transport and avoids threshold voltage fluctuation due to discrete, random dopant placement. In addition, if the interface trap concentration is very low (as it is desirable) Coulomb scattering could be neglected.

Figure 10 shows mobility curves versus the inversion charge concentration \( N_{inv} \) for two values of the silicon thickness: \( T_w = 2 \text{ nm} \), and \( T_w = 20 \text{ nm} \). Phonon and surface roughness scatterings have been taken into account according to the models described in Refs. 4 and 11. For surface roughness scattering, the following parameters have been considered for both interfaces:\(^{11,12}\) \( L_{sr} = 1.5 \text{ nm} \), \( \Delta_{sr} = 0.25 \text{ nm} \). Mobility curves corresponding to the symmetric-gate DGSOI inversion layer are shown in a solid line, while mobility curves corresponding to asymmetric gate devices are shown in a dashed line. These figures show that for the two values of \( T_w \), mobility curves for asymmetric devices are considerably below the mobility curves corresponding to symmetric devices, i.e., the difference between symmetric and asymmetric curves is bigger when surface roughness scattering is taken into account than when surface roughness scattering is ignored (as in Fig. 9). That means that surface roughness scattering is considerably stronger for asymmetric devices than for symmetric devices. In addition, in the case of the thinnest sample (\( T_w = 2 \text{ nm} \)), the surface roughness effect is important even at low inversion charge concentration. To see this more clearly, Fig. 11 shows again (no symbols, symmetric devices in solid line and asymmetric devices in dashed line) the same mobility curves of Fig. 10 for \( T_w = 2 \text{ nm} \), i.e., taking into account phonon and surface roughness scattering (\( L_{sr} = 1.5 \text{ nm} \), \( \Delta_{sr} = 0.25 \text{ nm} \)) and for the sake of comparison, mobility curves for the same devices (\( T_w = 2 \text{ nm} \), symmetric gate and asymmetric gate) but taking into...
account only phonon scattering (■), and taking into account phonon and surface roughness scattering but assuming a softer interface, i.e., $L_{sr} = 1.5$ nm, $\Delta_{sr} = 0.1$ nm (○). As observed, when only phonon scattering is taken into account mobility curves for both devices (symmetric and asymmetric) are very similar, according to the results of Fig. 9, and the discussions following Figs. 6–8 for $T_w < 3$ nm. However, when surface roughness scattering is taken into account mobility curves for asymmetric devices are strongly affected by the surface roughness scattering even at low inversion charge concentrations. This is a consequence of the shift of the inversion charge peak towards the $n^+$ gate shown in Fig. 5 for the asymmetric-gate case.

Coming back to Fig. 10, note that the two mobility curves corresponding to the thinnest sample ($T_w = 2$ nm) coincide for high values of the inversion charge concentration. In contrast, such a coincidence is not observed for the thickest sample, since the two mobility curves are very different even at high inversion charge concentrations. However, in thick samples (and at high inversion charge concentrations) symmetric DGSOI devices behave as two inversion layers connected in parallel. In addition, in asymmetric devices, only one channel will be formed for such a large $T_w$. Therefore we should compare electron mobility in the asymmetric channel, with the mobility in the symmetric device but with only half of the charge in the inversion layer, since the total charge is shared by two identical channels. Figure 12 compares the electron distribution in an asymmetric DGSOI inversion layer with $T_w = 20$ nm and $N_{inv} = 1 \times 10^{13} \text{cm}^{-2}$ (respectively, $N_{inv} = 2 \times 10^{13} \text{cm}^{-2}$) with the electron distribution of a symmetric DGSOI inversion layer with the same silicon thickness and exactly double the inversion charge concentration, i.e., $N_{inv} = 4 \times 10^{13} \text{cm}^{-2}$ (respectively, $N_{inv} = 4 \times 10^{13} \text{cm}^{-2}$). In the latter case, the charge is split between two identical channels, each of which has a charge...
FIG. 13. Evolution of electron mobility for a symmetric $n^+-n^+$ DGSOI (---) and an asymmetric $n^+-p^+$ DGSOI (-----) with the thicknesses of the silicon layer. Two different values of the inversion charge concentration were considered. Only phonon and surface-roughness scattering were taken into account.

FIG. 14. Ratio between electron mobility for a symmetric $n^+-n^+$ DGSOI and an asymmetric $n^+-p^+$ DGSOI with the thicknesses of the silicon layer.

We have studied electron mobility behavior in asymmetric-gate double-gate silicon on insulator silicon inversion layers, and compared it to the mobility in symmetric double-gate silicon on insulator devices. To do so, we examined the distribution of the electrons in both structures by self-consistently solving Poisson’s and Schroedinger’s equations in both structures. We show that the lack of symmetry in the former structures produces the loss of the volume inversion effect in asymmetric devices in the range 5 nm $< T_w < 25$ nm. This fact has important consequences for the electron transport properties in asymmetric devices. We show that in the range 5 nm $< T_w < 25$ nm.

(i) The conduction effective mass of electrons in asymmetric devices is lower than that of electrons in the symmetric case. This would contribute to an increase in electron mobility in the former devices.

(ii) The greater confinement of electrons in the asymmetric case, produced by the deeper potential well in the $n^+$ gate side, produces an increase in the phonon scattering rate. This would contribute to a decrease in the mobility in the asymmetric case.

However, for extremely thin devices, $T_w < 3$ nm, the two devices, symmetric gate and asymmetric gate have similar conduction effective mass and similar phonon scattering rate, although the electron distribution drifts slightly towards the $n^+$ gate.

We have solved the Boltzmann transport equation by the Monte Carlo method, and have evaluated the electron mobility, thus revealing the actual contribution of each of the above two effects on electron mobility, and the effect of the
surface roughness scattering. We have shown that the lack of symmetry, together with volume inversion, and the greater effect of surface roughness scattering, mean that the electron mobility in asymmetric DGSOI devices is considerably below the mobility curves corresponding to symmetric devices in the whole range of silicon thicknesses. The difference is greater in the range 5–25 nm, where electron mobility in symmetric DGSOI inversion layers is greatly improved by the volume inversion effect. We have shown that mobility in symmetric devices could be 2.5 times higher than that in their asymmetric counterparts.

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